1. (Amended) A memory system comprising:

a memory controller having an interface that includes a plurality of memory subsystem ports;

a first memory subsystem including:

a buffer device having a first port and a second port, and

a plurality of memory devices coupled to the buffer device via the second port, wherein data is transferred between at least one memory device of the plurality of memory devices and the memory controller via the buffer device;

and

a plurality of point-to-point links, each point-to-point link of the plurality of point-to-point links having a connection to a respective memory subsystem port of the plurality of memory subsystem ports, the plurality of point-to-point links including a first point-to-point link to connect the first port to a first memory subsystem port of the plurality of memory subsystem ports.

2. (Amended) The memory system of claim 1 further including:

a plurality of connectors, wherein each connector of the plurality of connectors is connected to a respective point-to-point link of the plurality of point-to-point links; and

a plurality of memory subsystems, and wherein each memory subsystem of the plurality of memory subsystems includes:

a buffer device having a first port and a second port, wherein the first port is coupled to a respective connector of

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the plurality of connectors; and

a plurality of memory devices coupled to the buffer device via the second port.

3. (Amended) The memory system of claim 2 further including a plurality of substrates wherein each memory subsystem of the plurality of memory subsystems is disposed on a respective substrate of the plurality of substrates.

4. (Amended) The memory system of claim 1 wherein the plurality of point-to-point links, first memory subsystem, and memory controller are disposed on a common substrate.

5. (Amended) The memory system of claim 1 wherein the first memory subsystem further includes a plurality of channels and a plurality of memory device select lines connected between the plurality of memory devices and the second port.

6. The memory system of claim 5 wherein each channel includes a plurality of terminated signal lines.

7. (Amended) The memory system of claim 1 wherein the buffer device of the first memory subsystem further includes a clock alignment circuit to generate an internal synchronizing clock signal having a predetermined timing relationship with a reference clock signal.

8. (Amended) The memory system of claim 1 further including a plurality of sideband signals coupled between the plurality of memory devices of the first memory subsystem and the memory

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controller.

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9. (Amended) The memory system of claim 1 further including a plurality of sideband signals coupled between the plurality of buffer devices and the memory controller.

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10. (Amended) A memory system comprising:

a controller device;

a first buffer device having a first interface and a second interface;

a second buffer device having a first interface and a second interface;

a first point-to-point link having a first connection to the controller device and a second connection to the first interface of the first buffer device;

a first plurality of memory devices connected to the second interface of the first buffer device;

a second point-to-point link having a first connection to the controller device and a second connection to the first interface of the second buffer device; and

a second plurality of memory devices connected to the second interface of the second buffer device.

11. The memory system of claim 10, wherein the first buffer device and first plurality of memory devices are disposed on a first substrate, and the second buffer device and second plurality of memory devices are disposed on a second substrate.

12. (Amended) The memory system of claim 11, further including:

a first plurality of signal lines to connect the first plurality of memory devices to the second interface of the first buffer device;

a second plurality of signal lines to connect the second plurality of memory devices to the second interface of the second buffer device;

a first plurality of termination elements connected to the first plurality of signal lines; and

a second plurality of termination elements connected to the second plurality of signal lines.

13. The memory system of claim 10, wherein the first buffer device further includes a third interface, the memory system further including:

a third buffer device having a first interface and a second interface;

a third point-to-point link having a first connection to the third interface and a second connection to the first interface of the third buffer device; and

a third plurality of memory devices connected to the second interface of the third buffer device.

14. The memory system of claim 10 further including a third point-to-point link having a connection to the controller and a fourth point-to-point link having a connection to the controller.

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15. (Amended) The memory system of claim 10 further including:

a first channel to connect the first plurality of memory devices to the second interface of the first buffer device;

a second channel to connect the second plurality of memory devices to the second interface of the second buffer device;

a third channel connected to the second interface of the first buffer device;

a third plurality of memory devices electrically coupled to the third channel;

a fourth channel connected to the second interface of the second buffer device; and

a fourth plurality of memory devices electrically coupled to the fourth channel.

16. The memory system of claim 15 further including:

a fifth and sixth channel connected to the second interface of the first buffer device;

a fifth plurality of memory devices electrically coupled to the fifth channel; and

a sixth plurality of memory devices electrically coupled to the sixth channel.

17. The memory system of claim 10, further including at least one termination element disposed on the first buffer device and electrically connected to the first point-to-point link.

18. (Amended) The memory system of claim 10 wherein the first and second buffer devices each further include a clock alignment

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circuit to generate an internal synchronizing clock signal having a predetermined timing relationship with a reference clock signal.

19. A memory system comprising:

a controller device;

a first and second plurality of buffer devices, each buffer device of the first and second plurality of buffer devices having an interface connected to a respective plurality of memory devices;

a first and second repeater device;

a first point-to-point link having a first connection to the controller device and a second connection to the first repeater device;

a second point-to-point link having a first connection to the controller device and a second connection to the second repeater device;

a first plurality of repeater links, each repeater link having a first connection to a respective buffer device of the first plurality of buffer devices, and a second connection to the first repeater device; and

a second plurality of repeater links, each repeater link having a first connection to a respective buffer device of the second plurality of buffer devices and a second connection to the second repeater device.

20. (Amended) The memory system of claim 19, wherein each buffer device of the first and second plurality of buffer devices and corresponding plurality of memory devices are each disposed on

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one of a plurality of respective module substrates.

21. (Amended) The memory system of claim 19 further including a third point-to-point link having an end connected to the controller device and a fourth point-to-point link having an end connected to the controller device.

22. (Amended) The memory system of claim 19 wherein each buffer device of the first and second plurality of buffer devices each further include a clock alignment circuit to generate an internal synchronizing clock signal having a predetermined timing relationship with a reference clock signal.

23. (Amended) A memory system comprising:

a controller device having an interface;

a first connector, second connector, and third connector;

a first point-to point link having a first connection to the interface and a second connection to the first connector;

a second point-to-point link having a first connection to the interface and a second connection to the second connector;

a third point-to-point link having a first connection to the interface and a second connection to the third connector; and

a first memory subsystem including:

a buffer device connected to the first connector; and

a plurality of memory devices connected to buffer device, wherein at least one memory device of the plurality of memory devices transfer data to the controller device via the buffer device.

24. (Amended) The memory system of claim 23 wherein the second and third connectors support coupling to respective second and third memory subsystems.

Please **ADD** the following claims:

25. (New) The memory system of claim 1 further including a second memory subsystem including:

a buffer device having a first port and a second port, wherein the first port is connected to a second point-to-point link of the plurality of point-to-point links; and

a plurality of memory devices coupled to the buffer device via the second port.

26. (New) The memory system of claim 1 wherein each memory device of the plurality of memory devices included in the first memory subsystem includes a dynamic random access memory cell array.

27. (New) The memory system of claim 1 further including a module substrate having a connector interface, wherein the first memory subsystem is disposed on the module substrate, and the buffer device is electrically connected to the connector interface, wherein the buffer device transceives data, control and address signals between the plurality of memory devices and the connector interface.

28. (New) The memory system of claim 27 further including a motherboard substrate having a socket which interfaces with the connector interface, wherein the memory controller and the plurality of point-to-point links are disposed on the motherboard substrate.

29. (New) The memory system of claim 1 further including first termination disposed on the buffer device and coupled to the first point-to-point link, to terminate a first end of the point-to-point link.

30. (New) The memory system of claim 29 further including second termination disposed on the memory controller and coupled to the first point to point link, to terminate a second end of the point-to-point link.

31. (New) The memory system of claim 1 wherein the buffer device communicates with the controller device over the first point-to-point link by encoding symbols using a number of signal levels, wherein the number of signal levels is greater than two.

32. (New) The memory system of claim 1 wherein the buffer device further includes a cache memory coupled to the first port, to store data being provided from the memory controller to at least one memory device of the plurality of memory devices.

33. (New) The memory device of claim 1 wherein the buffer device further includes a write buffer, coupled to the first port,

to hold data to be provided to at least one memory device of the plurality of memory devices.

34. (New) The memory system of claim 10 wherein each memory device of the first plurality of memory devices includes a dynamic random access memory cell array.

35. (New) The memory system of claim 10 further including a module substrate having a connector interface, wherein the first buffer device is disposed on the module substrate, and the first buffer device is electrically connected to the connector interface, and wherein the first buffer device transceives data, control and address information between the first plurality of memory devices and the connector interface.

36. (New) The memory system of claim 35 further including a motherboard substrate having a socket which interfaces with the connector interface, wherein the controller device and the first point-to-point link are disposed on the motherboard substrate.

37. (New) The memory system of claim 10 wherein the first buffer device communicates with the controller device over the first point-to-point link by encoding symbols using a number of signal levels, wherein the number of signal levels is greater than two.

38. (New) The memory system of claim 10 wherein the first buffer device further includes a cache memory, coupled to the first interface of the first buffer device, to store data being provided

from the controller device to at least one memory device of the first plurality of memory devices.

39. (New) The memory device of claim 10 wherein the first and second buffer device further includes a write buffer, coupled to the first interface of the first buffer device, to hold data to be provided to at least one memory device of the first plurality of memory devices.

40. (New) The memory system of claim 19 wherein each buffer device of the first and second plurality of buffer devices further includes a cache memory to store data being provided from the controller device to at least one memory device of the respective plurality of memory devices.

41. (New) The memory device of claim 19 wherein each buffer device of the first and second plurality of buffer devices further includes a write buffer to hold data to be provided to at least one memory device of the respective plurality of memory devices.

42. (New) The memory system of claim 23 wherein each memory device of the plurality of memory devices included in the first memory subsystem includes a dynamic random access memory cell array.

43. (New) The memory system of claim 23 further including a module substrate having a connector interface, wherein the first memory subsystem is disposed on the module substrate, and the buffer device is electrically connected to the connector interface,

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and wherein the buffer device transceives data, control and address signals between the plurality of memory devices and the connector interface.

44. (New) The memory system of claim 43 wherein the first connector is a socket which interfaces with the connector interface and wherein the memory system further includes a motherboard substrate, wherein the controller device, the socket, first, second and third point-to-point links are disposed on the motherboard substrate.

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45. (New) The memory system of claim 23 further including first termination disposed on the buffer device to terminate a first end of the point-to-point link.

46. (New) The memory system of claim 45 further including second termination disposed on the controller device to terminate a second end of the point-to-point link.

47. (New) The memory system of claim 23 wherein the buffer device communicates with the controller device over the first point-to-point link by encoding symbols using a number of signal levels, wherein the number of signal levels is greater than two.

48. (New) The memory system of claim 23 wherein the buffer device further includes a cache memory to store data being provided from the controller device to at least one memory device of the plurality of memory devices.

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49. (New) The memory device of claim wherein the buffer device further includes a write buffer to hold data to be provided to at least one memory device of the plurality of memory devices.

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